REMARKS/ARGUMENTS

After entry of this amendment, claims 1-31 will remain pending in this application.

Claims 1-7 stand rejected under 35 U.S.C 103(a) as being unpatentable over Miyanaga et al., United States patent number 5,514,893 (Miyanaga) in view of Verhaege et al., United States patent number 6,529,359 (Verhaege). Claim 8 stands rejected under 35 U.S.C 103(a) as being unpatentable over Miyanaga in view of Verhaege and Toyashima, United States patent application number 20010017755. Claims 9-16 stand rejected under 35 U.S.C 103(a) as being unpatentable over Miyanaga in view of Verhaege and Kwon, United States patent application number 20020163768. Claims 17-23 stand rejected under 35 U.S.C 103(a) as being unpatentable over Miyanaga in view of Verhaege and Toyashima and Sher, United States patent number 6,417,721. Claim 27 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Fugate et al., United States patent number 6,525,594 (Fugate) in view of Zhu et al., United States patent number 5,933,047 (Zhu). Reconsideration of these rejections in light of these remarks and allowance of the pending claims is respectfully requested.

Claim 1

Claim 1 stands rejected under 35 U.S.C 103(a) as being unpatentable over Miyanaga in view of Verhaege. But this combination of references do not show or suggest each and every element of this claim. For example, claim 1 recites "a resistor having a first terminal coupled to the pad, and a second terminal coupled to receive an input signal." Neither Miyanaga nor Verhaege provide this feature.

The pending office action cites Verhaege as providing this feature. (See pending office, page 3, first paragraph.) In particular, resistor Rout in Figure 1 of Verhaege is cited as showing a resistor having a first terminal coupled to a pad and a second terminal coupled to receive an input signal. But Verhaege's Rout does not have a first terminal coupled to a pad and a second terminal coupled to receive an input signal as required by the claim.

Rather, Verhaege shows a resistor Rout 38 having a first terminal coupled to an output driver including devices Pout 14 and Nout 12, and a second terminal coupled to a pad 36.

(See Verhaege, Figure 1 and column 2, lines 48-50.) The first terminal of Rout 38 is not coupled to receive an input signal. Also, given the topology, it is clear that if an input signal was to be received, it would be at the second terminal of Rout 38, since this pad is connected to a pad 36 that is labeled I/O. In this configuration, the same terminal of Rout 38 would be coupled to the pad and also coupled to receive an input signal. Accordingly, Verhaege does not show or suggest a resistor having a first terminal coupled to a pad and a second terminal coupled to receive an input signal as required by the claim.

Further, Miyanaga adds nothing to this, as it does not show or suggest the required resistor. Rather, Figure 1 of Miyanaga shows a resistor 6 having a first terminal connected to a pad to receive an input signal and a second terminal coupled to an input buffer 7. (See Miyanaga, Figure 1.) The same terminal is coupled to the pad and coupled to receive an input signal, different terminals are not coupled to the pad and coupled to receive an input signal. Accordingly, neither reference provides a resistor having a first terminal coupled to a pad and a second terminal coupled to receive an input signal as required by the claim.

Claim 1 further recites "an input buffer coupled between a first supply terminal and a second supply terminal and having an input directly connected to a pad." The cited references do not provide this feature.

The pending office action cites Miyanaga and Verhaege as providing this. (See pending office action, page 4, fourth paragraph.) But the input buffer in Miyanaga does not provide an input buffer having an input directly connected to a pad as required.

Rather, the input buffer 7 in Figure 1 of Miyanaga is connected to the pad through resistor 6. (See Miyanaga, Figure 1.) Accordingly, the input buffer 7 is not connected directly to the pad 1. Verhaege adds nothing as it does not show an input buffer.

Accordingly, the cited references do not show an input buffer having an input directly connected to a pad as required. It should also be noted that while Kwon shows a circuit device 220 connected to pad 210 (see Kwon, Figure 4), Miyanaga teaches away from using this arrangement as it would eliminate resistor 6 and the protection it provides for input buffer 7. (See Miyanaga, column 8, lines 20-22.)

For at least these reasons, claim 1 should be allowed.

Claim 17

Claim 17 stands rejected under 35 U.S.C 103(a) as being unpatentable over Miyanaga in view of Verhaege and Toyashima and Sher. However, it is not obvious to combine these four references.

The pending office action states that it is obvious to combine the buffer 7 of Figure 1 of Verhaege with the resistor 6 of Figure 1 of Miyanaga with the diode D1 of Figure 2 of Toyashima with the switch 30 of Figure 2E of Sher in the manner recited in the claim. (See pending office action, page 6, second paragraph.) The pending office action uses these four references to piece together the circuit elements recited in the claim. These four references are combined by impermissibly using hindsight. There is no motivation supplied for this in the references themselves. Rather, the references appear to suggest that they not be combined in this way.

For example, the switches in Sher are used to vary the load presented to a driving circuit for matching reasons. That is, if one pin is more loaded due to process tolerances, other pins can have their loads increased to match. (See Sher, abstract, column 1, line 58 to column 2, line 5.) It is not obvious to combine these switches with the protection circuit in Toyashima, which provides a different function. Rather, Toyashima teaches away from using switches.

The diodes D1 and D2 in Toyashima are in series with fuses F1 and F2. The diodes D1 and D2 in Figure 2 of Toyashima protect circuitry during packaging and transportation. When the integrated circuit is being used, the diodes D1 and D2 are disconnected by blowing the fuses F1 and F2. This removes the capacitance of the diodes D1 and D2 and allows high speed operation. (See Toyashima, abstract.) It is well known that a blown fuse provides a lower capacitance than an open MOS switch as shown in Sher. Thus, if switches were used in place of the fuses F1 and F2, the higher speed operation achieved by Toyashima would not be realized.

Also, Toyashima also teaches that blowing these fuses F1 and F2 eliminates the possibility of latch-up being caused by the diodes D1 and D2 during device operation. (See

Toyashima, paragraph 39.) This is because once the fuses F1 and F2 are blown, the silicon regions of the diodes D1 and D2 are not connected to the input terminal 10. If switches are used in place of the fuses F1 and F2, silicon regions of the switches would still be connected to the input terminal 10 when the switches were open. Accordingly, the immunity to latch-up achieved by Toyashima would not be realized if switches were used in place of the fuses F1 and F2.

Moreover, as described in Sher, switches require a control voltage. It is not simply a matter of blowing a fuse once, the control voltage needs to be maintained. (See Sher, column 5, lines 6-10.) Thus, the simplicity of design achieved by Toyashima would not be achieved if switches were used in place of the fuses F1 and F2.

Therefore, it is not obvious to combine the diode in Toyashima with the switch in Sher. Rather, since the speed improvement, latch-up immunity, and simplicity afforded by the fuses F1 in F2 in Toyashima would be compromised, Toyashima teaches away from using switches in place of these fuses.

For at least these reasons, claim 17 should be allowed.

Claim 27

Claim 27 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Fugate in view of Zhu. But this combination of references do not teach each and every element of this claim. For example, claim 27 recites "when the control signal is in a second state, the bulk of the pull-up transistor is coupled to the first supply voltage, and a drain-to-bulk diode of the pull-up transistor clamps a voltage received at the pad." These references do not provide this feature.

The pending office action cites Zhu as showing the transistor that couples the bulk of the pull-up transistor to the first supply voltage. (See pending office action, page 8, third paragraph.) But Zhu does not show or suggest clamping a voltage received at the pad as required by the claim.

Rather, Zhu provides a circuit for generating a voltage VPP that exceeds the voltage VDD. (See Zhu, column 2, lines 62-65 and Figure 5.) The voltage VPP is used in writing to memory cell capacitors in DRAM memories. (See Zhu, column 1, lines 20-39.)

Clamping this signal as claimed would reduce the voltage of VPP to that of VDD plus one diode drop. This would make the generation of a separate VPP voltage superfluous. It is therefore undesirable to clamp this voltage as required by the claim. Accordingly, Zhu does not show or suggest clamping a voltage received at the pad as required by the claim.

For at least this reason, claim 27 should be allowed.

Other claims

Claim 9 should be allowed for similar reasons as claim 1. The other claims depend on one of the above claims and should be allowed for at least the same reasons and for the additional limitations they recite.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal notice of allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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